WHAT IS CLAIMED IS:

1. A software program stored on a recordable medium, the software program being used for product culmination estimation in a semiconductor fabrication facility (fab), the software program comprising:

instructions for receiving a lot size for a product to be processed by a plurality of process events;

instructions for determining a theoretical cycle time (TCT) as a sum of processing times for the plurality of process events for the lot size;

instructions for determining a target queue time (TQT) as a function of a standard theoretical cycle time (STCT) and a standard queue time factor (QTF) assigned to the product, independent of lot size;

instructions for performing a product culmination estimation for the lot size of the product as a function of the TCT and the target queue time.

2. The software program of claim 1, wherein the function for product culmination estimation equals: TCT + TQT.

3. The software program of claim 1, wherein the function for determining TQT equals: QTF x STCT.

4. A method for product culmination estimation in a semiconductor manufacturing environment, comprising:

providing a manufacturing executing system comprising a plurality of processing entities and a plurality of computing entities, the manufacturing system providing interconnectivity and management of the processing entities and the computing entities;

assigning a standard queue time factor (QTF) to product advancing through the manufacturing executing system;

determining an actual theoretical cycle time (ATCT) associated with the product through each process entity of the manufacturing executing system;

anticipating a target queue time (TQT) for the product through the manufacturing executing system as a function of the ATCT and the QTF; and

forecasting a product cycle time of the product through the manufacturing executing system as a function of the TQT.

5. The method of claim 4 wherein the QTF is specific to a process flow.

6. The method of claim 4 wherein the QTF is specific to a portion of a process flow.

7. The method of claim 4 wherein the manufacturing executing system comprises a communications network, the network further coupled to a plurality of computing entities for determining the ATCT.

8. The method of claim 7 wherein the ATCT comprises a plurality of values, one for each processing entity.

9. The method of claim 4 wherein the manufacturing executing system comprises a communications network, the network further coupled to a plurality of computing entities for determining the TQT.

10. The method of claim 9 wherein the TQT comprises a plurality of values as a function of the plurality of ATCT and QTF, one for each processing entity.

11. The method of claim 9 wherein the QTF comprises a constant value common among the plurality of processing entities.

12. The method of claim 9 wherein the QTF comprises a plurality of constant values, one for each processing entity.

13. The method of claim 1 wherein the processing entities represents a single product process.

14. The method of claim 1 wherein the TQT comprises the product of the standard queue time factors and the theoretical cycle time.

15. The method of claim 14 wherein the TQT comprises a target queue time for a plurality of product through a plurality of processing entities.

16. The method of claim 1 wherein the product cycle time comprises the summation of the target queue time and the actual cycle time.

17. The method of claim 16 wherein the product cycle time comprises a product cycle time for a plurality of product through a plurality of processing entities.

18. The method of claim 1 wherein the product includes between about one and about twenty five semiconductor substrates, wherein the substrates have a diameter between about 200 mm and about 500 mm.

19. The method of claim 1 wherein the product includes a multiple project wafer, the multiple project wafer comprising a plurality of different product.

20. The method of claim 19 wherein the multiple project wafer includes a plurality of standard queue time factors.

21. A system for product culmination estimation in a microelectronics manufacturing environment, the system comprising:

a first group of instructions for establishing a manufacturing executing system having a plurality of processing entities and a plurality of computing entities;

a second group of instructions for providing a product culmination estimator, the product culmination estimator being a function of a plurality of standard queue time factors assigned to the products in the manufacturing system, an actual and theoretical cycle time, a target queue time, and a product cycle time; and

one or more memories for storing the first or second group of instructions.

22. The system of claim 21 wherein the standard queue time factors are specific to a process flow.

23. The system of claim 21 wherein the standard queue time factors are specific to a portion of a process flow.

24. The system of claim 21 wherein the manufacturing executing system comprises a communications network, the network further coupled to a plurality of computing entities for determining the actual theoretical cycle time.

25. The system of claim 24 wherein the actual theoretical cycle time comprises a plurality of values, one for each processing entity.

26. The system of claim 21 wherein the manufacturing executing system comprises a communications network, the network further coupled to a plurality of computing entities for determining the target queue time.

27. The system of claim 26 wherein the target queue time comprises a plurality of values as a function of the plurality of actual theoretical cycle time and queue time factors, one for each processing entity.

28. The system of claim 21 wherein the manufacturing executing system comprises a communications network, the network further coupled to a plurality of computing entities for determining the product cycle time.

29. The system of claim 21 wherein the manufacturing executing system comprises a communications network, the network further coupled to a plurality of computing entities for assigning the queue time factor to the product through the manufacturing executing system.

30. The system of claim 29 wherein the queue time factor comprises a constant value common among the plurality of processing entities.

31. The system of claim 29 wherein the queue time factor comprises a plurality of constant values, one for each processing entity.

32. The system of claim 21 wherein the processing entities represents a single product process.

33. The system of claim 21 wherein at least one of the processing entities is a batch product process.

34. The system of claim 21 wherein the target queue time comprises the product of the standard queue time factors and the theoretical cycle time.

35. The system of claim 34 wherein the target queue time comprises a target queue time for a plurality of product through a plurality of processing entities.

36. The system of claim 21 wherein the product cycle time comprises the summation of the target queue time and the actual cycle time.

37. The system of claim 36 wherein the product cycle time comprises a product cycle time for a plurality of product through a plurality of processing entities.

38. The system of claim 21 wherein the product includes between about one and about twenty five semiconductor substrates, wherein the substrates have a diameter between about 200 mm and about 500 mm.

39. The system of claim 21 wherein the product includes a multiple project wafer, the multiple project wafer comprising a plurality of different product.

40. The system of claim 39 wherein the multiple project wafer includes a plurality of standard queue time factors.